EE/CprE/SE 491 WEEKLY REPORT 4

Date: ***Feb 20th, 2023 – February 26th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

For the fourth week, we mainly tested more of the open-source software and tried to understand more of the analog process flow and how it fits into the Efabless process. A major breakthrough was made as there was a branch that was made that fixed the Makefiles for the analog Caravel example/template project. After some testing, we were able to get it working and fully simulate the chip and run prechecks on it. This breakthrough is huge, as this has been a roadblock for the last month.

Past week accomplishments

- Joshua Thater
    - Created documentation outlining how to create the environment needed to run all of the tools and fully simulate/precheck the chip
    - Created a fresh VM to be shared with other team members that have all the needed tools on it
    - Simulated and ran precheck on analog sample project
- Aiden Petersen
    - Got caravel analog framework functioning
    - Research into analog caravel wrapper
- Matt Ottersen
    - Worked on getting digital simulations to work

    - Researched layout tools and process
- Regassa Dukele
    - Researched layout integration process.
    - Designed and did some simulations for basic analog components.

Pending issues

- How do we generate a .gds file
- Linerging questions remain about how the whole analog design flow fits into Efabless process and tools
- Getting analog sample project to pass prechecks

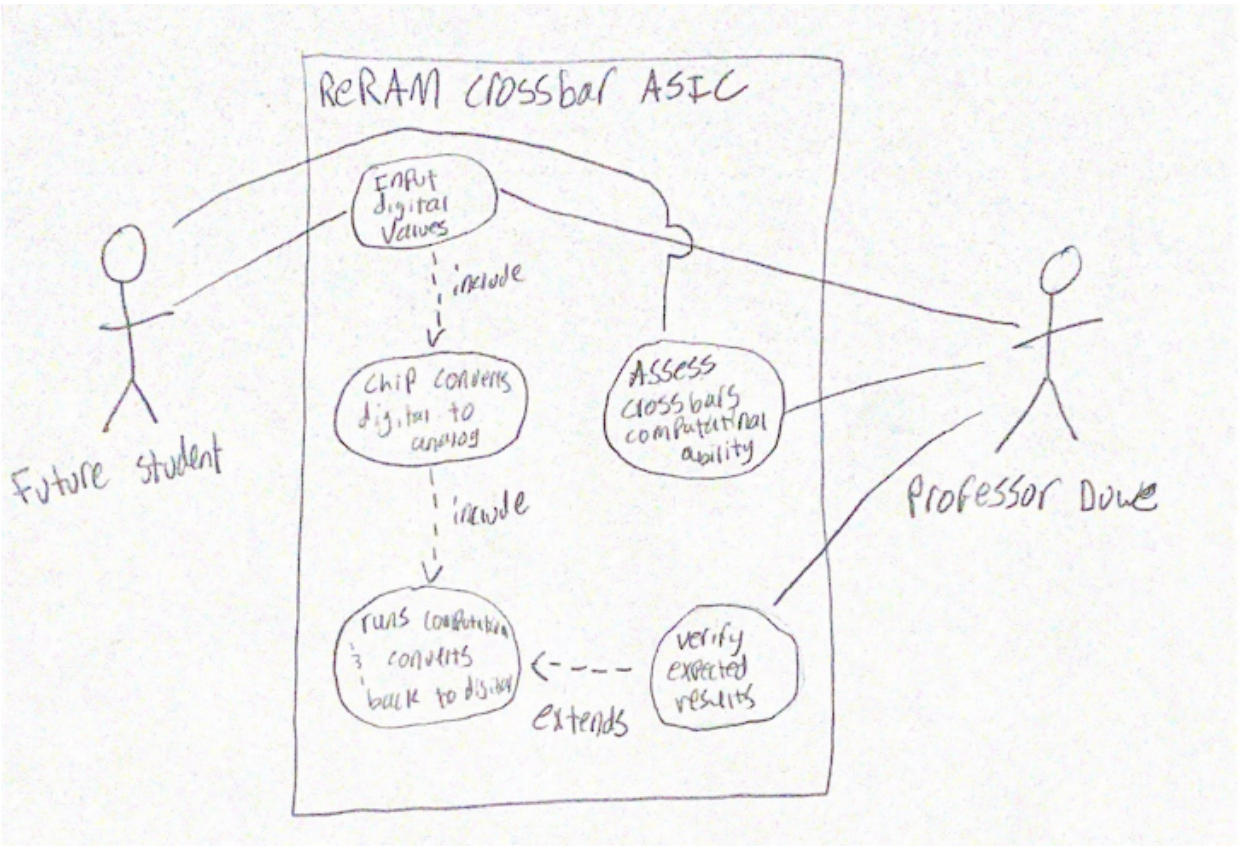
Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Created test environment, and documentation	7	27
Aiden Petersen	Caravel framework works!	4	25
Matt Ottersen	Research on digital simulation and layout tools/process	6	21
Regassa Dukele	Researched layout integration process	5	21.5

Plans for the upcoming week

- Joshua Thater
    - Fully simulate and precheck a sample analog project
    - Learn how to generate a .gds file
    - Continue to write out documentation on the analog process
- Aiden Petersen
    - Better understand and document how to use the caravel framework
    - Create flowchart of tooling
- Matt Ottersen
    - Simulate a digital circuit and then create a layout of it
- Regassa Dukele
    - Make schematic and run simulation.

Use Case Diagram:


ReRAM crossbar ASIC
Input digital values
include
Chip converts digital to analog
include
Runs computation & converts back to digital
Assess crossbars computational ability
Verify expected results
extends
Future student
Professor Duke